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LLNL-CONF-559280

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May 31, 2012

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Oakland, CA, United States
May 14, 2012 through May 17, 2012

Disclaimer

Current reduction of CdZnTe via band gap engineering

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***Abstract* — CdZnTe-based gamma detectors require a reduction of electronic noise contributed by apparent device and surface leakage current, especially for advanced readout schemes such as the Co-planar Grid or Pixelated Grid. In this work, we describe a combination of surface treatments and amorphous semiconductor layers that result in a reduction of both apparent device and surface leakage current compared to metal contacts on Br:MeOH etched devices. Characterization by scanning electron microscopy (SEM), spectroscopic ellipsometry (SE), x-ray photoelectron spectroscopy (XPS), current-voltage (IV), and pulse height spectra is performed.**

***Index Terms* — CdZnTe, radiation detection, gamma spectroscopy, amorphous semiconductors**

I. Introduction

Improved processing and surface preparation techniques are required to increase the spectroscopic performance of CdZnTe gamma detectors [1-6]. Apparent device and surface leakage current generated by surface electronic properties contributes to the noise and limits ultimate detector performance [7-10]. These issues are pronounced at the gamma energies energies below 200 keV, which is a region evaluated for ^{235}U and ^{239}Pu, amongst others. Fig. 1 qualitatively shows the sources of noise vs gamma energy calculated for a planar CZT detector including trapping of both electron and holes. Electronic noise, or apparent device leakage current, dominates at these energies. In addition, advanced readout schemes such as co-planar grids [5] and pixelated detectors [6] with steering grids achieve the best performance but are limited by surface currents generated by voltage differentials between elements on the same surface.

This work describes efforts to control both the apparent device and surface leakage current through the application of surface treatments in combination with amorphous semiconducting layers between the CZT and the metal electrode. Characterization of these treatments and amorphous layers is performed using a variety of techniques.

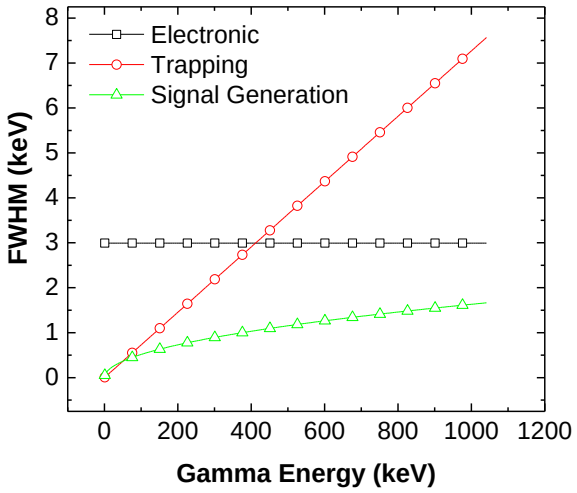

Fig. 1. Sources of noise for CZT gamma detectors

II. Preparation of CZT Surface

A. Removal of polishing damage

CZT crystals were grown and polished by Redlen Technologies. As received, the crystals were subjected to varying plasma treatments involving H_2 and Ar as well as metallization schemes including a-Si and a-Se, which are similar to those described later in this work. The IV characteristics were shown to be strongly face dependent, with no change of the IV possible through the use of surface treatments or varying contact schemes, shown in Fig. 2.

It is well known that even careful surface polishing induces a layer of damage known as the Beilby layer. It was deduced that this layer was controlling the IV characteristics of the crystals. Removal of this layer can be accomplished by a 30s dip in 2% Br:MeOH, a common treatment in the fabrication of CZT gamma detectors. Fig. 3 shows the absorption coefficient of the CZT crystals measured by spectroscopic ellipsometry

Manuscript received June 01, 2012; revised January 10, 2013; accepted February 07, 2013. This work was performed under the auspices of the U.S. DOE by Lawrence Livermore National Laboratory under contract DE-AC52-07NA27344, LLNL-CONF-559280. This work was supported by the Defense Threat Reduction Agency, Basic Research Department.

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(SE) both before and after etching with 2% Br:MeOH. Note that before etching, the CZT shows a gradual change in absorption near the band edge. This indicates a large absorption tail that extends into the band gap of the CZT crystal, a sign of significant damage and sub-band states. The presence of this damaged layer is likely the reason the IV characteristics cannot be changed (Fig. 2), as the damage layer controls the transport properties at the CZT/metal interface. After etching, a sharp absorption edge is observed, indicating a crystalline surface. This surface is expected to allow for control over the transport properties.

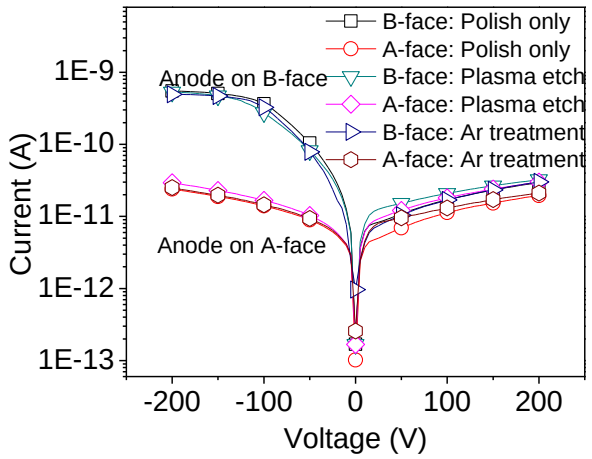


Fig. 2. IV for various surface treatments on unetched CZT.

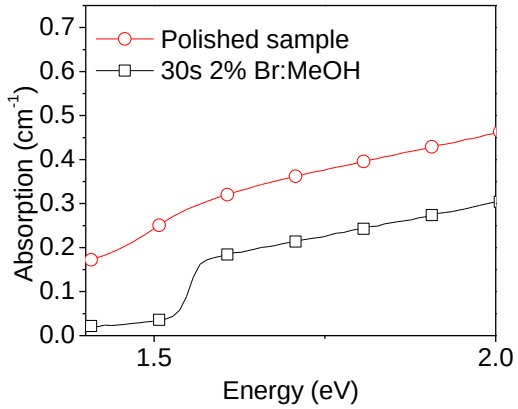


Fig. 3. Absorption coefficient measured by SE for CZT before and after etching in 2% Br:MeOH

B. *Plasma treatments to control surface termination*

After damage removal, it is still desirable to modify the surface properties. This is because it is well known that Br:MeOH treatments leave the surface Te rich, which may not be optimal. In order to achieve control over the surface termination, we have developed a series of plasma treatments which allow for changing of the surface termination over a wide range of Cd:Te ratios measured by XPS, shown in Table I.

Plasma etching was performed in an Electron Cyclotron Resonance (ECR) high density plasma etcher. The high density plasma produced in an ECR results in a large ion flux to the surface with relatively low ion energy, which results in low damage to the treated surface. Etching was performed at 3 mTorr with a 400W RF power (-200V DC Bias), 850W (130A) ECR Source power, and 60/10/30 sccms of $Ar/CH_4/H_2$. The Ar acts to preferentially remove Cd relative to Te [10] while the H_2 acts to remove Te in the form of volatile TeH_2. The addition of CH_4 is common in this type of gas chemistry and may aid in the formation of volatile Cd byproducts. This etch chemistry provides a balance between the removal of Cd, Zn, and Te and

TABLE I
SURFACE CD:TE RATIOS

Treatment	Cd:Te ratio
Polished only	1.47
2% Br:MeOH	0.59
45s $Ar/H_2/CH_4$ etch	1.06

results in a smooth surface with an etch rate of 0.25 µm/min. As shown in Table I, it leaves the surface near stoichiometric. A time of 45s was chosen in order to ensure removal of the Te rich surface layer produced by Br:MeOH etching. Although not shown, the absorption measured by SE is essentially unchanged from the case of Br:MeOH etching alone.

III. DEPOSITION OF AMORPHOUS LAYERS

A. *Selection of amorphous semiconductors*

The use of amorphous semiconductors to decrease dark current has previously been reported for Ge detectors [11]. Selection of appropriate amorphous semiconductor layers has the potential to allow for a higher barrier to electron and hole injection compared with metal only contacts without compromising signal collection. Candidates must include the correct band offsets, such that they act as barriers to injection into the CZT while at the same time no barrier exists for transport from the CZT into the metal electrode. Two potential candidates that fit this criteria are a-Si for use as an electron barrier and a-Se for use as a hole barrier. Fig. 4 shows theoretical band lineups of these materials using band gaps and electron affinities taken from the literature [12-14].

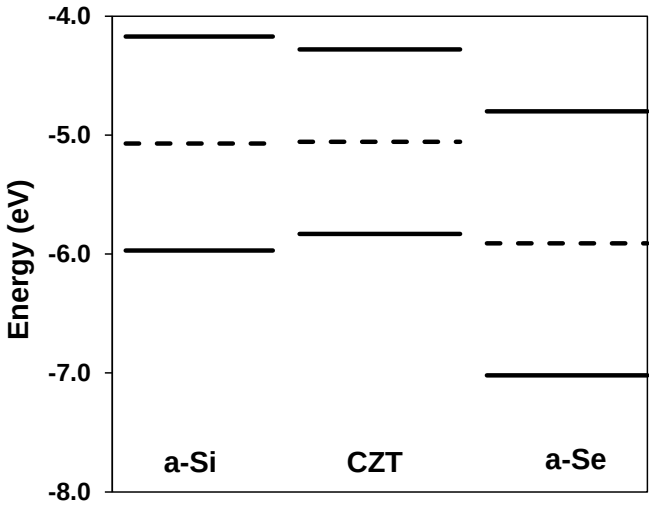
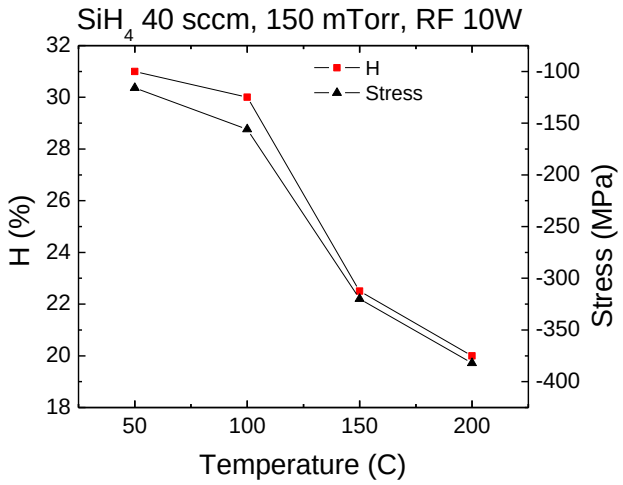


Fig. 4. Theoretical band lineup for a-Se and a-Si compared with CZT for separated semiconductors

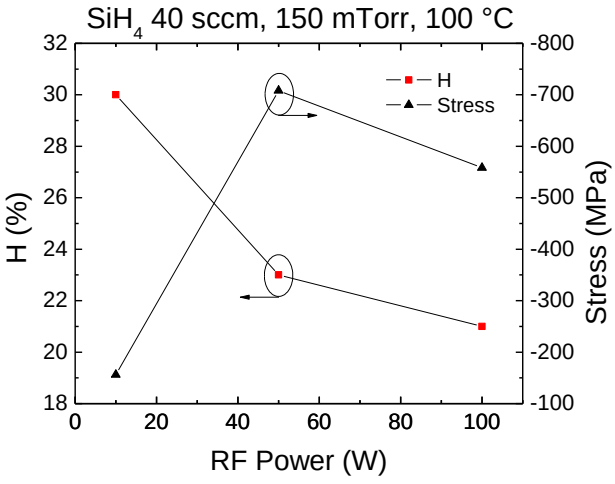
In addition to potentially increased barriers to injection, amorphous layers have the potential to provide other benefits. These include reduced surface leakage current, due to their high resistivity, and improved contact uniformity. These likely depend on the deposition conditions of the amorphous layers, as well as on the CZT surface preparation prior to amorphous layer deposition. This is because the band lineup at the interface between the amorphous layer and the CZT is affected by the CZT surface Fermi level, which will determine whether the leakage current is able to flow through the relatively conductive CZT surface layer or the more resistive amorphous semiconductor.

B. Deposition and characterization of a-Si

Deposition of a-Si was accomplished with Plasma Enhanced Chemical Vapor Deposition (PECVD) using pure SiH_4 as the precursor gas. Depositions were carried out at 150 mTorr with a SiH_4 flow of 40 sccm. The temperature and RF power were varied in order to find conditions which produced a low stress film with high H content, as measured by Rutherford Backscattering (RBS). These results are shown in Figure 5a and 5b.



a)



b)

Fig. 5. Hydrogen content and stress of a-Si for a variety of deposition conditions, a) substrate temperature and b) RF power.

This demonstrates that a low temperature and low RF power are required to achieve large H concentrations with low stress. H incorporation in a-Si improves the electronic transport [16], while low stress is necessary to ensure adhesion to the CZT. It should be noted that because CZT is very temperature sensitive, performing the deposition at a temperature greater than 150°C would not be desirable. The chosen deposition conditions for use on CZT were 50°C, 25W RF, 40 sccm SiH_4, and 150 mTorr. A slightly higher RF power was chosen due to instabilities in the plasma. This resulted in non-uniformities in the film, measurable by SE. At 25W, the non-uniformity was measured to be <5%.

Fig. 6 shows the absorption coefficient k measured by SE and fit with the Cody-Lorentz model, which is known to be appropriate for amorphous semiconductors. The fitting is excellent, with a mean square error (MSE) of < 0.5 (where < 2.50 is considered good). The extracted band gap for this is measured to be 1.941 eV, which is similar to that reported for PECVD deposited a-Si. The small increase in the band gap compared to true value for a-Si is likely due to a small amount of oxygen contamination.

The bulk resistivity of the a-Si was measured using the transmission line method (TLM) with Au contacts. A resistivity >5 x 10^{10} Ω-cm was observed.

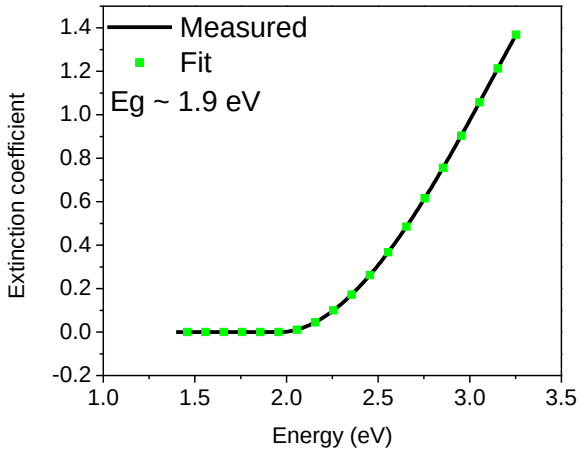


Fig. 6. Absorption coefficient vs energy for amorphous Si on crystalline Si.

C. Deposition and characterization of a-Se

Amorphous Se was deposited via resistively heated thermal evaporation using 99.999% pure Se pellets. A base pressure of 3 x 10^{-6} torr was achieved in the chamber prior to deposition. Because Se is known to be hazardous, a special fixture was fabricated to prevent contamination of the vacuum chamber. This consists of a cylindrical tube 3" in diameter which extends from the deposition boat up to the substrate holder. This tube can be removed and sequestered if necessary.

In addition to the tube, a heat sink was placed on the backside of the substrate holder in order to prevent overheating of the sample during deposition. This is critical

because pure a-Se is known to crystallize at temperatures >60°C, which are easily achievable in a thermal evaporation system. Crystallized Se has a high conductivity compared to a-Se and is undesirable our application. Indeed, without the heat sink, the quality of the film was significantly compromised. Figure 7 shows SEM micrographs of amorphous and crystallized Se deposited on Si substrates.

After deposition, the band gap of the a-Se was measured via SE and fit with the Cody-Lorentz model. An excellent fit was achieved, with an MSE < 0.5, shown in Fig. 8. The extracted band gap was measured to be 2.017 eV, in good agreement with reported values in the literature [12]. TLM patterns were deposited on the a-Se with Au contacts. Similar to the case of a-Si, a resistivity > 5 x 10^{10} Ω-cm was observed.

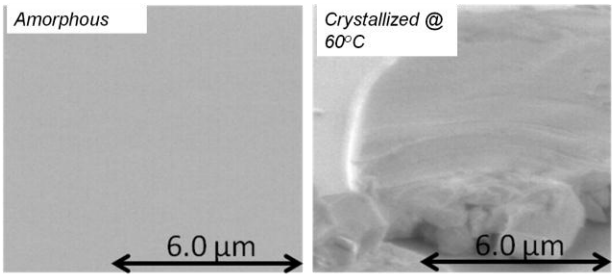


Fig. 7. SEM micrographs of amorphous and crystallized Se layers

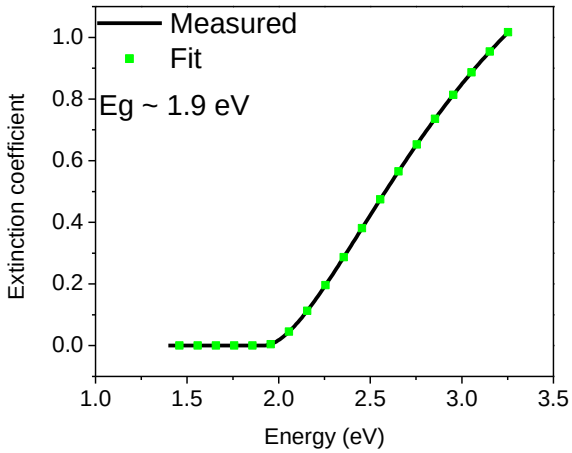


Fig. 8. Absorption coefficient vs energy for amorphous Se on crystalline Si

IV. DEVICE PERFORMANCE

A. Device preparation

Devices were prepared using a combination of the surface preparation steps and amorphous layers discussed. CZT crystals 10x10x5 mm^3 were used for the study. A pixelated readout scheme with guard ring but without steering grid was used. Initially, devices were fabricated with pixels on each side in order to measure the surface leakage current. After initial electrical testing, a blanket layer of Al was deposited on one side of selected devices in order to perform radiation measurements. Pixels were 1 mm x 1 mm with 250 µm spacing. Four devices were fabricated, described in Table II.

TABLE II
FABRICATED DEVICES

Device #	Surface preparation	Anode	Cathode
1	Polish	Au	Al
2	Br:MeOH	Au	Al
3	Br:MeOH	Au/a-Si	Al/a-Se
4	Br:MeOH + Plasma etch	Au/a-Si	Al/a-Se

B. Surface leakage current

Surface leakage current was measured on each device between pixels. Figure 9 shows (a) the effect of a-Si and (b) the effect of a-Se. Also included in the figures is the surface leakage current for polished crystals with metal electrodes. Note that the final surface preparation step prior to amorphous layer deposition has a strong impact on the surface leakage current. This is likely due to modulation of the CZT surface Fermi level due to changes in the surface termination.

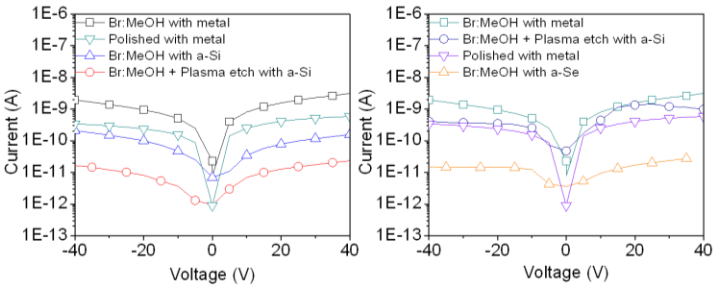


Fig. 9. Surface leakage current (L) with an amorphous Si layer and (R) with an amorphous Se layer

Interestingly, a-Si and a-Se show opposite effects. In the case of a-Si, a final treatment of Br:MeOH results in significantly increased surface leakage current as compared to the polished device, while the plasma etch results in a 100x decrease in the surface leakage current. For a-Se, the opposite effect is seen. The device treated with Br:MeOH displays the lowest surface leakage current. This is likely due to the change of the surface Fermi level and band bending at the CdZnTe/amorphous layer interface.

C. Apparent device leakage current

Apparent device leakage current was measured for selected devices as well, shown in Fig. 10. Note the use of Br:MeOH before metal layer deposition results in a significant increase in leakage current as compared to the samples that did not have the Br:MeOH treatment. The use of a-Si and a-Se decreases the leakage current to a level comparable to that observed for the polished devices. For the plasma etched sample, leakage current with a positive applied bias is increased; however a decrease is observed for negative applied bias.

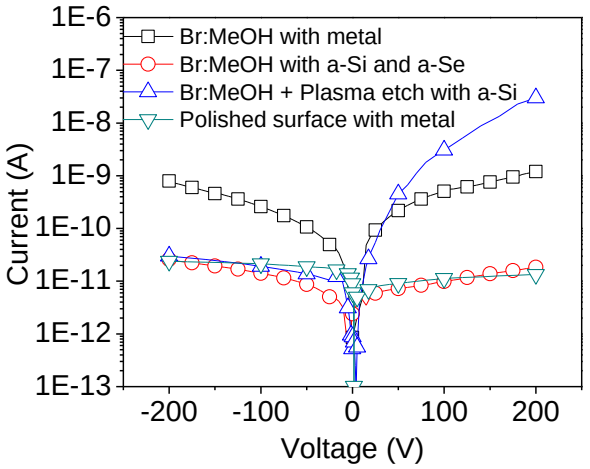
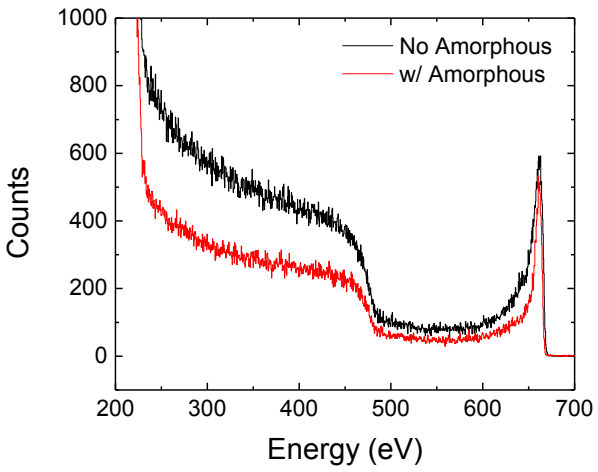
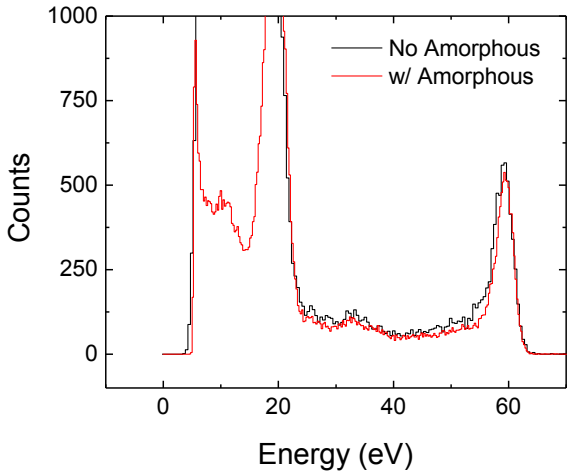


Fig. 10. Apparent device leakage current



a)



b)

Fig. 11. ^{137}Cs (a) and ^{241}Am (b) response with and with out amorphous layers.

D. Gamma response

For gamma measurements, blanket Al was deposited on the side which already received Al for devices 2 and 3. IV measurements were performed through the sample in order to confirm that no adverse effects were induced by further processing. Devices were packaged in an electrical probe fixture with the planar contact negatively biased, the measured pixel and guard ring grounded, and the other 3 pixels unconnected due to limitation with the measurement setup. These devices were irradiated from the planar contact side with source distance adjusted to prevent pile-up. The detected gamma signal was read out from one pixel through an Amptek A250 charge preamplifier circuit and an Ortec 673 spectroscopy amplifier with 0.5 µs shaping time.

Measurement of spectra for both the 60 keV ^{241}Am line and the 662 keV ^{137}Cs line was performed. Fig. 11 shows the spectra taken at 500V for each source. Differences in total counts are likely due to variations in the distance from the source to the detector. The resolution is improved with the addition of the amorphous layers in both cases from 2.36% to 1.02% for ^{137}Cs (Fig. 11a) and from 7.27% to 5.92% for ^{241}Am (Fig. 11b). Note that for the 662 keV line, the tail of the photopeak is reduced and the ratio of the photopeak to the Compton edge is increased from 1.26 to 2 with the additional amorphous layers, while the pulser width remains constant or is slightly degraded. These are indications of reduced electrical noise and improved charge collection with the use of amorphous layers.

V. CONCLUSIONS

This work demonstrates the potential of improved surface preparation in combination with amorphous semiconductor layers to improve CZT performance for gamma spectroscopy. The ability to modify the surface termination of CZT is shown via plasma processing and the techniques to deposit high quality a-Si and a-Se are demonstrated. Further, it is shown that apparent device leakage current can be slightly improved while surface leakage current can be radically reduced compared to polished and/or Br:MeOH treated surfaces. This is dependent on the precise surface termination of the CdZnTe crystal as well as the type of amorphous layer used.

This work shows the potential for careful surface preparation and surface science to impact the state of the art performance for CZT detectors. Future work will address the question of surface termination more precisely, improve the deposition quality of amorphous films, and incorporate the use of steering grids on the pixels to demonstrate the effect of reduced surface leakage current.

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